

CLAIMS

What is claimed is:

- 1    1.    A method for designing an integrated circuit (IC), said method comprising:  
2            compiling a hardware description language (HDL) code to produce a  
3                    technology independent RTL (register transfer level) netlist;  
4            allocating a portion of an area of said IC to a specific portion of said  
5                    technology independent RTL netlist.
- 1    2.    A method as in claim 1 wherein said allocating restricts circuitry created from  
2            said specific portion to said portion of said IC.
- 1    3.    A method as in claim 1 further comprising:  
2            mapping said technology independent RTL netlist to a selected technology  
3                    architecture.
- 1    4.    A method as in claim 3 wherein said IC comprises one of a programmable  
2            logic device or an Application Specific IC (ASIC).
- 1    5.    A method as in claim 3 wherein said mapping is performed after said  
2            allocating.
- 1    6.    A method as in claim 3 further comprising:

2 performing a place and route operation after said mapping to implement said  
3 IC in said selected technology architecture.

1 7. A method as in claim 3 further comprising:  
2 optimizing a design of said IC after said allocating.

1 8. A method as in claim 7 wherein said optimizing optimizes said IC by removing  
2 duplicative logic or input/outputs.

1 ~~10~~ 9. A method as in claim 3 wherein said HDL code is created without regard to  
2 said allocating.

1 ~~9~~ 10. A method as in claim 7 wherein said optimizing and said mapping are  
2 performed after said allocating.

1 11. A method as in claim 3 further comprising:  
2 mapping portions of said technology independent RTL netlist to a selected  
3 technology architecture wherein estimates of IC resources are obtained  
4 from said mapping portions and wherein said mapping portions is  
5 performed after said compiling and before said mapping.

1 ~~13~~ 12. A method as in claim 3 further comprising:

2 optimizing interconnects between modules of said technology independent  
3 RTL netlist before said allocating.

1 <sup>12</sup> 13. A method as in claim 11 wherein said estimates are used to decide how to  
2 perform said allocating.

1 14. A method as in claim <sup>12</sup> 13 wherein a user considers said estimates and selects a  
2 command to decide how to perform said allocating.

1 15. A method as in claim 3 wherein said IC comprises a programmable logic  
2 device and wherein said method further comprises:  
3 testing a prototype of a system with said IC;  
4 performing a synthesis of said HDL code to generate at least one Application  
5 Specific Integrated Circuit (ASIC).

1 16. A method as in claim 3 further comprising:  
2 partitioning said technology independent RTL netlist between representations  
3 of said IC and another IC.

1 17. A method as in claim 16 wherein said partitioning is performed before said  
2 mapping.

1 18. A method as in claim 16 further comprising:

2 selecting logic designed for placement on one of said IC and said another IC  
3 and replicating said logic for placement on the other of said IC and said  
4 another IC.

1 19. A method as in claim 16 further comprising:  
2 selecting one RTL component in said technology independent RTL netlist and  
3 splitting said one RTL component into a first RTL component designed  
4 for placement on said IC and a second RTL component designed for  
5 placement on said another IC.

1 <sup>23</sup><sub>20</sub>. A digital processing system for use in designing an integrated circuit (IC), said  
2 digital processing system comprising:  
3 a display device;  
4 a memory;  
5 a processor coupled to said memory and to said display device, said processor  
6 allocating a specific portion of a technology independent RTL (register  
7 transfer level) netlist to a portion of said IC, said technology  
8 independent RTL netlist being stored in said memory.

1 <sup>24</sup><sub>21</sub>. A digital processing system as in claim <sup>23</sup><sub>20</sub> wherein said processor compiles a  
2 hardware description language (HDL) code to produce said technology independent  
3 RTL netlist and wherein said allocating restricts circuitry created from said specific  
4 portion to said portion of said IC.

1 <sup>25</sup>~~22~~. A digital processing system as in claim <sup>24</sup>~~21~~ wherein said IC comprises one of a  
2 programmable logic device or an ASIC.

1 <sup>26</sup>~~23~~. A digital processing system as in claim <sup>24</sup>~~21~~ wherein said processor maps said  
2 technology independent RTL netlist to a selected technology architecture.

1 <sup>27</sup>~~24~~. A digital processing system as in claim <sup>24</sup>~~23~~ wherein said processor maps said  
2 technology independent RTL netlist after said processor performs said allocating.

1 <sup>27</sup>~~25~~. A digital processing system as in claim <sup>24</sup>~~23~~ wherein said processor performs a  
2 place and route operation after said processor maps said technology independent RTL  
3 netlist, wherein said place and route operation creates a representation of circuitry in  
4 said selected technology architecture.

1 <sup>28</sup>~~26~~. A digital processing system as in claim <sup>27</sup>~~24~~ wherein said processor optimizes a  
2 design of said IC after said processor performs said allocating.

1 <sup>30</sup>~~27~~. A digital processing system as in claim <sup>27</sup>~~23~~ wherein said processor maps said  
2 technology independent RTL netlist after said processor performs said allocating.

1 <sup>31</sup>~~28~~. A digital processing system as in claim <sup>30</sup>~~27~~ wherein said processor maps  
2 portions of said technology independent RTL netlist to said selected technology

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3 architecture to generate estimates of IC resources and wherein said processor maps  
4 said portions after said processor compiles said HDL code.

1 <sup>32.</sup><sub>29.</sub> A digital processing system as in claim <sup>30</sup><sub>27</sub> wherein said processor displays  
2 said estimates on said display device and stores said estimates in said memory.

1 <sup>33.</sup><sub>30.</sub> A digital processing system as in claim <sup>32</sup><sub>29</sub> wherein said processor displays  
2 graphical representations of the area of said IC on said display device and displays on  
3 said display device representations of portions of said technology independent RTL  
4 netlist and wherein said processor performs said allocating in response to a command  
5 from a user.

1 <sup>34.</sup><sub>31.</sub> A digital processing system as in claim <sup>33</sup><sub>30</sub> wherein estimates of area  
2 requirements of said portions of said technology independent RTL netlist are  
3 displayed on said display device.

1 <sup>35.</sup><sub>32.</sub> A machine readable medium containing a plurality of executable instructions,  
2 which when executed on a digital processing system cause said digital processing  
3 system to perform a method for designing an integrated circuit (IC), said method  
4 comprising:  
5 compiling an hardware description language (HDL) code to produce a  
6 technology independent RTL (register transfer level) netlist;

7 allocating a portion of an area of said IC to a specific portion of said  
8 technology independent RTL netlist.

1 <sup>34.</sup>~~33.~~ A machine readable medium as in claim <sup>35</sup>~~32~~ wherein said allocating restricts  
2 circuitry created from said specific portion to said portion of said IC.

1 <sup>36.</sup>~~34.~~ A machine readable medium as in claim <sup>35</sup>~~32~~, wherein said method further  
2 comprises:  
3 mapping said technology independent RTL netlist to a selected technology  
4 architecture.

1 <sup>37.</sup>~~35.~~ A machine readable medium as in claim <sup>38</sup>~~34~~ wherein said IC comprises one of a  
2 programmable logic device or an ASIC.

1 <sup>40.</sup>~~36.~~ A machine readable medium as in claim <sup>38</sup>~~34~~ wherein said mapping is performed  
2 after said allocating.

1 <sup>41.</sup>~~37.~~ A machine readable medium as in claim <sup>38</sup>~~34~~, said method further comprising:  
2 performing a place and route operation after said mapping to implement said  
3 IC in said selected technology architecture.

1 <sup>44.</sup>~~38.~~ A machine readable medium as in claim <sup>38</sup>~~34~~, said method further comprising:  
2 optimizing a design of said IC after said allocating.

1 <sup>45.</sup>~~39.~~ A machine readable medium as in claim <sup>44</sup>~~38~~ wherein said optimizing optimizes  
2 said IC by removing duplicative logic or input/outputs.

1 <sup>42.</sup>~~40.~~ A machine readable medium as in claim <sup>38</sup>~~34~~ wherein said HDL code is created  
2 without regard to said allocating.

1 <sup>46.</sup>~~44.~~ A machine readable medium as in claim <sup>44</sup>~~38~~ wherein said optimizing and said  
2 mapping are performed after said allocating.

1 <sup>52.</sup>~~42.~~ A machine readable medium as in claim <sup>38</sup>~~34~~, said method further comprising:  
2 mapping portions of said technology independent RTL netlist to a selected  
3 technology architecture wherein estimates of IC resources are obtained  
4 from said mapping portions and wherein said mapping portions is  
5 performed after said compiling and before said mapping.

1 43. A machine readable medium as in claim <sup>38</sup>~~34~~, said method further comprising:  
2 optimizing interconnects between modules of said technology independent  
3 RTL netlist before said allocating.

1 <sup>53.</sup>~~44.~~ A machine readable medium as in claim <sup>52</sup>~~42~~ wherein said estimates are used to  
2 decide how to perform said allocating.

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1 <sup>54.</sup>~~45.~~ A machine readable medium as in claim <sup>53</sup>~~44~~ wherein a user considers said  
2 estimates and selects a command to decide how to perform said allocating.

1 <sup>51.</sup>~~46.~~ A machine readable medium as in claim <sup>38</sup>~~34~~ wherein said IC comprises a  
2 programmable logic device and wherein said method further comprises:  
3 testing a prototype of a system with said IC;  
4 performing a synthesis of said HDL code to generate at least one Application  
5 Specific Integrated Circuit (ASIC).

1 47. A machine readable medium as in claim <sup>38</sup>~~34~~, said method further comprising:  
2 partitioning said technology independent RTL netlist between representations  
3 of said IC and another IC.

1 48. A machine readable medium as in claim 47 wherein said partitioning is  
2 performed before said mapping.

1 49. A machine readable medium as in claim 47, said method further comprising:  
2 selecting logic designed for placement on one of said IC and said another IC  
3 and replicating said logic for placement on the other of said IC and said  
4 another IC.

1 50. A machine readable medium as in claim 47, said method further comprising:

2 selecting one RTL component in said technology independent RTL netlist and  
3 splitting said one RTL component into a first RTL component designed  
4 for placement on said IC and a second RTL component designed for  
5 placement on said another IC.

1 <sup>55.</sup>~~51.~~ A system for designing an integrated circuit (IC), said system comprising:  
2 means for compiling a hardware description language (HDL) code to produce  
3 a technology independent RTL (register transfer level) netlist;  
4 means for allocating a portion of an area of said IC to a specific portion of said  
5 technology independent RTL netlist.

1 <sup>56.</sup>~~52.~~ A system as in claim <sup>55</sup>~~51~~ wherein said allocating restricts circuitry created from  
2 said specific portion to said portion of said IC.

1 <sup>57.</sup>~~53.~~ A system as in claim <sup>55</sup>~~51~~ further comprising:  
2 means for mapping said technology in dependent RTL netlist to a selected  
3 technology architecture.

1 <sup>58.</sup>~~54.~~ A system as in claim <sup>57</sup>~~53~~ wherein said IC comprises one of a programmable  
2 logic device or an ASIC.

1 <sup>59.</sup>~~55.~~ A system as in claim <sup>57</sup>~~53~~ wherein said mapping is performed after said  
2 allocating.

1 <sup>60.</sup>~~56.~~ A system as in claim <sup>57</sup>~~53~~ further comprising:  
2 means for performing a place and route operation after said mapping to  
3 implement said IC in said selected technology architecture.

1 <sup>71.</sup>~~57.~~ A system as in claim <sup>57</sup>~~53~~ further comprising:  
2 means for optimizing a design of said IC after said allocating.

1 <sup>72.</sup>~~58.~~ A system as in claim <sup>71</sup>~~57~~ wherein said optimizing optimizes said IC by  
2 removing duplicative logic or input/outputs.

1 <sup>61.</sup>~~59.~~ A system as in claim <sup>57</sup>~~53~~ wherein said HDL code is created without regard to  
2 said allocating.

1 <sup>73.</sup>~~60.~~ A system as in claim <sup>71</sup>~~57~~ wherein said optimizing and said mapping are  
2 performed after said allocating.

1 <sup>62.</sup>~~61.~~ A system as in claim <sup>57</sup>~~53~~ further comprising:  
2 means for mapping portions of said technology independent RTL netlist to a  
3 selected technology architecture wherein estimates of IC resources are  
4 obtained from said mapping portions and wherein said mapping  
5 portions is performed after said compiling and before said mapping.

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10.  
1 ~~62.~~ A system as in claim ~~55~~<sup>51</sup> further comprising:  
2 means for optimizing interconnects between modules of said technology  
3 independent RTL netlist before said allocating.

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1 63. A system as in claim ~~61~~<sup>62</sup> wherein said estimates are used to decide how to  
2 perform said allocating.

1 64. A system as in claim 63 wherein a user considers said estimates and selects a  
2 command to decide how to perform said allocating.

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1 65. A system as in claim ~~55~~<sup>51</sup> wherein said IC comprises a programmable logic  
2 device and wherein said system further comprises:  
3 means for testing a prototype of a system with said IC;  
4 means for performing a synthesis of said HDL code to generate at least one  
5 Application Specific Integrated Circuit (ASIC).

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1 66. A system as in claim ~~55~~<sup>51</sup> further comprising:  
2 means for partitioning said technology independent RTL netlist between  
3 representations of said IC and another IC.

1 67. A system as in claim 66 wherein said partitioning is performed before said  
2 mapping.

1 68. A system as in claim 66 further comprising:  
2 means for selecting logic designed for placement on one of said IC and said  
3 another IC and replicating said logic for placement on the other of said  
4 IC and said another IC.

1 69. A system as in claim 66 further comprising:  
2 means for selecting one RTL component in said technology independent RTL  
3 netlist and splitting said one RTL component into a first RTL  
4 component designed for placement on said IC and a second RTL  
5 component designed for placement on said another IC.

1 <sup>20</sup>~~70.~~ A method as in claim 1 further comprising:  
2 selecting logic designed for placement in one of said area of said IC and  
3 another area of said IC and replicating said logic for placement on the  
4 other of said area and said another area.

1 <sup>37.</sup>~~71.~~ A machine readable medium as in claim <sup>35</sup>~~32~~, said method further comprising:  
2 selecting logic designed for placement in one of said area of said IC and  
3 another area of said IC and replicating said logic for placement on the  
4 other of said area and said another area.

1 <sup>21.</sup>~~72.~~ A method as in claim 1 further comprising:

2 selecting one RTL component in said technology independent RTL netlist and  
3 splitting said one RTL component into a first RTL component designed  
4 for placement in said area of said IC and a second RTL component  
5 designed for placement in another area of said IC.

1 <sup>22.</sup>~~73.~~ A machine readable medium as in claim <sup>21</sup>~~72~~, said method further comprising:  
2 selecting one RTL component in said technology independent RTL netlist and  
3 splitting said one RTL component into a first RTL component designed  
4 for placement in said area of said IC and a second RTL component  
5 designed for placement in another area of said IC.

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